What is claimed is:

1. A PLL comprising:

a phase comparator for comparing a reference frequency of an external clock signal with a comparison frequency of a comparison clock signal;

a filter for filtering an output signal from the phase comparator;

a VCO for generating a clock signal of frequency proportional to a DC signal from the filter;

a prescaler for selectively dividing the output clock signal from the voltage control oscillator by using at least two or more division ratios;

a program counter for dividing an output signal from the prescaler with a predetermined division ratio, and outputting the comparison clock signal having the comparison frequency;

a swallow counter for controlling the division ratio of the prescaler; and

a controller for outputting a control signal to control frequency division of the VCO by using set points of the prescaler, the swallow counter and the program counter.

2. The PLL according to claim 1, wherein the prescaler is set at large one of the two or more division ratios while the swallow counter operates.

3. The PLL according to claim 2, wherein the prescaler is set at small one of the two or more division ratios when the swallow counter counts a pulse by the set point.

4. The PLL according to claim 2, wherein the controller is a decoder.

5. The PLL according to claim 4, wherein the decoder is configured using the bit number of output bits, the whole counter set point, the swallow counter set point and the program counter set point.

6. The PLL according to claim 5, wherein the bit number of output signal is determined by determining voltage profit of the VCO when the set point of the prescaler is set,

wherein the whole counter set point of corresponding frequency is determined, wherein the swallow counter set point and the program counter set point corresponding to the whole counter set point are determined.